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CLAIMS

Having thus described my invention, what I claim as new and desire to secure by Letters Patent is as follows:

1. A method of adjusting carrier mobility in
 2 semiconductor devices comprising the steps of

depositing a first stressed film on a wafer including first and second transistors to create a stress in the channels of the transistors,

partially removing said first stressed film to relieve said stress from a channel of one said transistor,

depositing a second stressed film over first and second transistors to apply a second stress to the channel of the transistor having said first stressed film removed.

- 2. A method as recited in claim 1 in which first
 transistor and second transistor are of different
 conductivity types.
- 3. A method as recited in claim 2 in which first film and second film apply opposing stresses.
- 4. A method as recited in claim 3 wherein the carrier mobility is regulated by applying tensile stress to said first transistor while applying compressive stress to said second transistor.
- 5. A method as recited in claim 4 wherein at least one stressed film is applied using plasma enhanced chemical vapor deposition (PECVD).

- 1 6. A method as recited in claim 4 wherein at least
- 2 one stressed film is applied using thermal chemical
- 3 vapor deposition (CVD).
- 1 7. A method as recited in claim 5 wherein at least
- one stressed film is applied using thermal(CVD).
- 1 8. A method as recited in claim 4 further
- 2 comprising the steps of:
- 3 partially or fully removing first stressed film
- 4 from both first and second transistors as masked by
- 5 an oxide layer;
- 6 removing said oxide layer and depositing a
- 7 shear force isolation layer across entire CMOS pair;
- applying a blocking layer to first transistor
- 9 and associated portions of said layers/films;
- 10 removing layer/film portions associated with
- 11 said second transistor;
- 12 removing said blocking layer from said first
- 13 transistor; and
- 14 depositing said second stressed film over the
- 15 first and second transistors.
- 1 9. A method as recited in claim 4 further
- comprising the steps of:
- 3 applying a blocking layer to said first
- 4 transistor;
- 5 partially or fully removing said first stressed
- 6 film from second transistor;
- 7 removing said blocking layer from said first
- 8 transistor; and
- 9 applying said second stressed film over the
- 10 first and second transistors.

- 1 10. A structure that adjusts carrier mobility in 2 CMOS transistors comprising:
- 3 a substrate,
- a first transistor having a gate dielectric,
- gate electrode, and source, drain, and gate silicide
- 6 regions, formed on said substrate,
- a second transistor having a gate dielectric, gate electrode, and source, drain, and gate silicide regions, formed on said substrate,
- a first film providing tensile stress at least at the channel of first transistor,
- 12 a second film providing compressive stress at
- 13 least at the channel of second transistor, and
- 14 a shear force isolation layer separating said
- first film and said second film in at least one
- 16 area.
 - 1 11. A structure as recited in claim 10 wherein the
 - 2 first and second films can be composed of nitride,
 - 3 oxide, or other material that exhibits either
 - 4 tensile or compressive properties.
 - 1 12. A structure as recited in claim 11 wherein the
 - 2 first and second stressed films are separated by a
 - 3 shear force isolation layer at all points.
 - 1 13. A structure as recited in claim 12 wherein the
 - 2 first stressed film, closer to the substrate than
 - 3 the second stressed film, does not fully surround
 - 4 the nMOS transistor, but rather the sides only,
 - 5 while the remaining surfaces of the nMOS transistor
 - 6 are contacted by said shear force isolation layer.

- 1 14. A structure as recited in claim 13 wherein said
- 2 shear force isolation layer is the only separation
- 3 between the nMOS transistor and said second film.
- 1 15. A structure as recited in claim 13 wherein said
- 2 shear force isolation layer surrounds the majority
- of the oxide liner of the pMOS transistor gate
- 4 electrode except the top of the gate which engages
- 5 directly with said second stressed film.
- 1 16. A structure as recited in claim 11 wherein the
- 2 first and second stressed films are separated by a
- 3 shear force isolation layer at selected areas.
- 1 17. A structure as recited in claim 16 wherein the
- 2 first stressed film, closer to the substrate than
- 3 the second stressed film, fully surrounds the nMOS
- 4 transistor.
- 1 18. A structure as recited in claim 17 wherein said
- 2 first stressed film is the only separation between
- 3 the nMOS transistor and said second stressed film.
- 1 19. A structure as recited in claim 17 wherein said
- 2 second stressed film surrounds the oxide liner at
- 3 the sides of the pMOS transistor gate electrode with
- 4 the top of the gate directly engaged with said
- 5 second stressed film.